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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,270	09/18/2001	Christopher J. Chevallier	703.019US3	8702

21186 7590 05/19/2004

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EXAMINER	
WOJCIECHOWICZ, EDWARD JOSEPH	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,270	CHEVALLIER, CHRISTOPHER J.	
	Examiner	Art Unit	
	Edward J Wojciechowicz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-55,57-69,72 and 75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *38-48,52-54,65-69,72 and 75* is/are allowed.

6)☒ Claim(s) *22,23,27,28,30-34,49,50,55,57,61 and 62* is/are rejected.

7)☒ Claim(s) *24-26, 29, 35-37, 51, 58-60, 63, and 64* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

A new, non-final action is given in this application. Applicant informed the PTO that the PTO-892 form identifying the reference, along with a copy of the reference, cited in the previous action was inadvertently omitted from the correspondence sent to applicant. Unfortunately, the examiner only became aware of applicant's request to supply the missing reference and restart the period for response, during the time when the examiner was physically relocating to the new PTO facility, and the application was unavailable to the examiner. This new action is given in response to applicant's amendment filed on 3-8-04.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 22, 23, 27, 28, 30-34, 49, 50, 55, 57, 61, and 62 are rejected under 35 U.S.C. 102(a) as being anticipated by Tobita (5,646,516). The reference to Tobita teaches the basic inventive concept and structure of the invention whereby an input voltage is reduced by applying the voltage to the source of an FET and deriving an output at the drain of the FET where the output voltage is reduced by the threshold voltage of the FET.

See, for example, the circuit of Fig. 7, along with the discussion at col. 14, l. 1-15, and equation (17) in col. 14 of Tobita. It is seen that output voltage V0 is the input voltage V30, at node 30, minus VTN31, which is the threshold voltage of transistor Q31. It is seen that the drain of transistor Q31 is also coupled to the well that bounds the transistor, as claimed.

In claims 32 and 34, the "region" is read as the well region.

The circuit arrangement recited in claims 49 and 55 is met by the circuit shown in Fig. 8 of Tobita. Where the input voltage can be reduced by the sum of the threshold voltages of a pair of transistors, as

claimed. For example, the input voltage Vcc is reduced at node 3 by the combined threshold voltages of transistors Q6 and Q3. See, the discussion at col. 15, l.1-10, and equation (20) in col. 15.

Allowable Subject Matter

Claims 24-26, 29, 35-37, 51, 58-60, 63, and 64 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 38-48, 52-54, 65-69, 72, and 75 are allowed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward J Wojciechowicz whose telephone number is 571-27-1739. The examiner can normally be reached on Monday through Wednesday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edward J Wojciechowicz
Primary Examiner
Art Unit 2815

EW: ew

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 22-77, as amended, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention, for the reasons given in the previous action, hereby incorporated by reference. As stated in the previous rejection, the exact method by which the voltage is reduced is not clearly defined. Rather than being a question of the scope of the claims, the claim fail to particularly point out and distinctly claim the inventive means by which the voltage reduction is achieved other than what is inherently produced by all transistors of the type described.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 22-77 are further rejected under 35 U.S.C. 102(a) as being anticipated by Tobita. The reference to Tobita appears to show the inventive process by which an initial voltage is reduced by the amount of a threshold voltage of a field effect transistor, and subsequently applied to a well surrounding the transistor and to an external circuit.

For example, comparing applicant's claim 22 method with the description of Tobita's Fig. 7 embodiment, it is seen that Tobita also applies a voltage to the first source/drain and gate of transistor Q31 at node (30) and that a voltage reduced by the threshold voltage of the transistor is provided at a second source/drain of the transistor and to the well bounding the transistor, as claimed. See, also, the discussion at col. 14, lines 1-15 of Tobita, as well.

The output voltage at node (2) of Tobita would also be applied to another circuit element or to an additional transistor as shown in Fig. 9 of Tobita, with transistor Q5 outputting to transistor Q1, and the surrounding well.

The Tobita reference also shows the various claimed modifications to the basic circuit arrangement described above, and specifically recognizes the advantages of providing a reduced voltage by utilizing the inherent reduction of input voltage by the threshold voltage of the transistor to which it is applied. All or the claimed method of operating steps, insofar as understood, would appear to be met by the Tobita reference.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward J Wojciechowicz whose telephone number is 703-308-4898. The examiner can normally be reached on Monday through Wednesday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-872-9317.

Edward J Wojciechowicz
Primary Examiner
Art Unit 2815

EW: ew

EDWARD WOJCIECHOWICZ
PRIMARY EXAMINER
GROUP 2500